Amendments to the Claims

Please amend claims 1, 18 and 20 as follows:

1. (Currently Amended) A transmission line tap circuit comprising:

at least two input terminals configured for coupling to a transmission line;

impedance load circuitry configured to provide an impedance load to the transmission line for tapping the transmission line and receiving a transmission signal propagating there through;

amplifying circuitry configured to amplify the received transmission signal and directly connected to the impedance load circuitry;

impedance matching circuitry configured to provide an impedance match to an impedance load of at least one Line Interface Unit (LIU) and directly connected to a plurality of outputs of the amplifying circuitry; and

at least two output terminals configured for coupling said transmission signal to the at least one LIU and directly connected to the impedance matching circuitry.

2. (Original) The circuit according to Claim 1, wherein the circuitry configured to provide the impedance load to the transmission line, the circuitry configured to amplify the received transmission signal, and the circuitry configured to provide the impedance match to the impedance load of the at least one LIU are provided within a single stage.

3. (Original) The circuit according to Claim 1, wherein the circuitry configured to provide the impedance load to the transmission line includes at least two resistors where a first of the at least two resistors is connected to a first of the at least two input terminals and a second of the at least two resistors is connected to a second of the at least two input terminals.

4. (Original) The circuit according to Claim 1, further comprising circuitry configured to block direct current present in the received transmission signal.

5. (Original) The circuit according to Claim 4, wherein the circuitry configured to block direct current includes at least a first capacitor connected to a first of the at least two input terminals and a second capacitor connected to a second of the at least two input terminals.

6. (Original) The circuit according to Claim 1, further comprising circuitry configured to provide a dissipation load for the received transmission signal.

7. (Original) The circuit according to Claim 6, wherein the circuitry configured to provide a dissipation load for the received transmission signal includes at least two resistors connected in series and coupled to the at least two input terminals.

8. (Original) The circuit according to Claim 1, further comprising circuitry configured to suppress noise in the received transmission signal and to shape the received transmission signal.

9. (Original) The circuit according to Claim 8, wherein the circuitry configured to suppress noise in the received transmission signal and to shape the received transmission signal includes at least two capacitors connected in series and coupled to the at least two input terminals.

10. (Original) The circuit according to Claim 1, wherein the circuitry configured to amplify the received transmission signal includes circuitry configured to wave shape the received transmission signal, at least two amplifiers each having respective feedback resistors, and at least two capacitors in parallel to a respective one of the feedback resistors.

11. (Original) The circuit according to Claim 1, further comprising circuitry configured to provide a dissipation load to the circuitry configured to amplify the received transmission signal.

12. (Original) The circuit according to Claim 11, wherein the circuitry configured to provide a dissipation load is in parallel to the circuitry configured to amplify the received transmission signal and includes at least two resistors connected in series.

13. (Original) The circuit according to Claim 1, further comprising circuitry configured to block direct current from the circuitry configured to amplify the received transmission signal.

14. (Original) The circuit according to Claim 13, wherein the circuitry configured to block direct current includes at least two capacitors connected in series and coupled to the at least two output terminals.

15. (Original) The circuit according to Claim 1, wherein the transmission line is a T1 transmission line.

16. (Original) The circuit according to Claim 1, wherein the transmission line is a E1 transmission line.

17. (Original) The circuit according to Claim 1, further comprising gain adjustment circuitry configured to adjust the gain of the circuit.

18. (Currently Amended) A method for interfacing a transmission line with at least one Line Interface Unit (LIU), the method comprising the steps of:

providing an impedance load to the transmission line for tapping the transmission line and receiving, via at least two input terminals, a transmission signal propagating there through;

amplifying the received transmission signal via amplifying circuitry directly connected to the impedance load;

providing an impedance match to an impedance load of the at least one LIU via direct connection from a plurality of outputs of the amplifying circuitry; and

providing, via at least two output terminals, the amplified signal to the at least one LIU.

19. (Original) The method according to Claim 18, further comprising the steps of:

blocking direct current present in the received transmission signal;

providing a dissipation load for the received transmission signal; and

suppressing noise in the received transmission signal.

20. (Currently Amended) A transmission line tap circuit comprising:

means for providing an impedance load to a transmission line for tapping the transmission line and receiving, via at least two input means, a transmission signal propagating there through;

means for amplifying the received transmission signal, such means being directly connected to the impedance load; and

means for providing an impedance match to an impedance load of at least one Line Interface Unit (LIU) for providing, via at least two output means, the amplified signal to the at least one LIU, such that the impedance match is directly connected to a plurality of outputs of the means for amplifying.